#14 Appeal Brief 9/30/00

PATENT
P54766

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Geun-Woo PARK

Serial No.: 08/922,300 Examiner: M. Marc-Coleman

Filed: 2 September 1997 Art Unit: 2774

For: DISPLAY DEVICE WITH POWER INTERRUPTION DELAY FUNCTION

Appeal No._____

The Honorable Commissioner
of Patents & Trademarks
Washington, D.C. 20231

ATTENTION: Board of Patent Appeals and Interferences

APPELLANT'S BRIEF (37 CFR §1.192)

This brief is in furtherance of the Notice of Appeal filed in this case on 25 July 2000.

The fees required under §1.17(f) for the filing of the Appellant's Brief are dealt with in the accompanying transmittal letter.

This brief is transmitted in triplicate (37 CFR §1.192(a)).

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APPEAL BRIEF

I. STATEMENT OF REAL PARTY IN INTEREST

Pursuant to 37 CFR §1.192(c)(1) the real party in interest is:

SamSung Electronics Co., Ltd.
416 Maetan-dong, Paldal-ku,
Suwon City, Kyungki-do,
Republic of Korea

II. RELATED APPEALS AND INTERFERENCES

Pursuant to 37 CFR §1.192(c)(2), there are no appeals nor interferences known to the Appellant, the Appellant's legal representative, or the Assignee (real party of interest) which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-4 have been finally rejected and are appealed herein; claims 5-7 have been objected to as being based upon a rejected base claim; and claims 8-11 have been allowed.

IV. STATUS OF AMENDMENTS AFTER FINAL REJECTION

No amendment has been filed after receipt of the final rejection.

V. SUMMARY OF THE INVENTION

Page 10, line 5 - Page 13, line 11

Fig. 3 is a detailed circuit diagram illustrating the construction of a display device with a power interruption delay function in accordance with the present invention. In the display device of Fig. 3, the voltage source V1 is connected to the input terminal of the H/V processor constant voltage circuit 131 through the power interruption delay charging circuit 370.

The power interruption delay charging circuit 370 includes a reverse voltage prevention diode D1 having its anode connected to the voltage source V1 and its cathode connected to the input terminal of the H/V processor constant voltage circuit 131, and a polarity capacitor C1 having its positive pole connected to a connection point of the cathode of the reverse voltage prevention diode D1 and the input terminal of the H/V processor constant voltage circuit 131 and its negative pole connected to the ground voltage terminal.

The operation of the display device with the above-mentioned construction in accordance with the present invention will hereinafter be described in detail.

When the display device is powered on, the high voltage from the high voltage source B+ is charged on the horizontal deflection coil H-DY and S-correction capacitor Cs through the field effect transistor FET1 and pulse transformer PT in the current amplifier 136 and then discharged through the discharge loop including the horizontal output transistor TR in the horizontal output circuit 134. Such charging and discharging operations are repeated as stated previously with reference to Fig. 2.

If the power supply to the display device is interrupted during the operation of the display

device, the voltage supply to the H/V processor constant voltage circuit 131 is at once stopped in the display device of Fig. 2, as shown in Fig. 4a. However, according to the present invention, a voltage, charged on the polarity capacitor C1 during the power supply, is applied to the input terminal of the H/V processor constant voltage circuit 131, as shown in Fig. 4b, while it is discharged. As a result, the H/V processor constant voltage circuit 131 does not immediately stop the voltage supply to the H/V processor 132.

Noticeably, the reverse voltage prevention diode D1 is connected in series between the voltage source V1 and the H/V processor constant voltage circuit 131 to protect the power supply circuit by allowing the voltage charged on the polarity capacitor C1 not to be discharged to the voltage source V1 at the power interruption state.

Because the voltage charged on the polarity capacitor C1 is continuously applied to the H/V processor constant voltage circuit 131 until it is completely discharged, the voltage supply to the H/V processor 132 is not interrupted immediately. Therefore, the H/V processor 132 outputs the horizontal pulse signal continuously for a predetermined time period, as shown in Fig. 5b.

The continuous pulse output time of the H/V processor 132 is determined according to a discharge time of the polarity capacitor C1. As a result, the continuous pulse output time of the H/V processor 132 can be varied by adjusting the discharge time of the polarity capacitor C1.

While the output pulse from the H/V processor 132 maintains such a high voltage level as to continuously drive the field effect transistor FET2 in the horizontal driver 133, the horizontal drive transformer T2 continues to be excited to induce a voltage in its secondary coil, thereby causing the horizontal output transistor TR in the horizontal output circuit 134 to remain at its driven

state. Hence, the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs can be sufficiently discharged. Namely, the discharge time of the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs is sufficient.

As apparent from the above description, according to the present invention, the power interruption delay charging circuit is provided at the input terminal of the H/V processor constant voltage circuit in the display device. The power interruption delay charging circuit can prevent the horizontal output transistor from being damaged due to an instantaneous surge current when power supply is resumed after power interruption. Further, the power interruption delay charging circuit can prevent the peripheral devices and circuits from being successively damaged due to damage in the horizontal output transistor.

VI. ISSUES

Whether claims 1-4 are patentable under 35 U.S.C. §103(a) over Applicant's admitted prior art in view of Hamaguchi et al. (*hereafter:* Hamaguchi).

VII. GROUPING OF CLAIMS

Claim 1 stands or falls alone, and claims 2-4 stand or fall with claim 1.

VIII. ARGUMENT

Claims 1-4 are not obvious and unpatentable under 35 U.S.C. §103(a) in view of the combined teachings of Applicant's admitted prior art and Hamaguchi et al. (*hereafter:* Hamaguchi).

The Applicant respectfully traverses this rejection for the following reason(s).

Applicant's admitted prior art comprises all that is claimed in claim 1 except the feature of *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted,* which is deemed to be non-obvious in view of the proposed combination of art.

It noted here that the Examiner has not identified where the foregoing feature of claim 1 is found in the applied art. Note, 37 CFR §1.104(c)(2) which directs the Examiner to designate the particular part relied on as nearly as practicable, when a reference is complex or shows or describes inventions other than that claimed by the applicant. Also note that he pertinence of each reference, if not apparent, must be clearly explained. *Ex parte Levy*, 17 USPQ2d 1461, 1462 (1990) states:

> "it is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference."

The Examiner relies on other case law, see paragraph 7 on pages 6-7 of Paper No. 8, to suggest that the references need not explicitly **provide motivation** for combining the teachings thereof, and to further suggest that the "examiner may provide an explanation based on logic and sound scientific reasoning that will support a holding of obviousness." The Examiner has **not** provided any sound scientific reasoning nor logical explanation of how the combination of references teach the feature of*power interruption delay charging means for gradually lowering said*

input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted. The Applicant has not argued the issue of motivation to combine Applicant's admitted prior art and Hamaguchi. The Applicant readily admitted:

> "There is no doubt that Hamaguchi's power regulatory circuitry would protect the CRT display of the Applicant's admitted prior art" (page 3, lines 8-9 of the response filed 1/7/00)

The Applicant, however, argues that the combination would not protect the CRT display by *gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted*, and the Examiner has not identified where this aspect of the claimed invention is taught by the combined art. The Examiner appears to be confusing **motivation** and **limitations**. The Examiner fails to identify any case law which permits the Office to ignore limitations of the claims, because there is no such case law.

In re Ochiai, 71 F.3d 1565, 37 USPQ2d 1127 (Fed. Cir. 1995):

> "The test for obviousness *vel non* is statutory. It requires that one compare the claim's 'subject matter as a whole' with the prior art 'to which said subject matter pertains.' 35 U.S.C. §103. The inquiry is thus highly fact-specific by design."

On page 6 of Paper No. 8 the Examiner states, "Hamaguchi et al. does not have to explicitly said that 'gradually lowering said input voltage'. Since circuit 16 of Hamaguchi et al. is equivalent to the power interruption circuitry claimed by the applicant." The Examiner is correct that Hamaguchi does not have to explicitly state "gradually lowering said input voltage," however the

art **must** provide some teaching to suggest to one of ordinary skill in the art the feature of *gradually lowering said input voltage.* The Examiner errs in stating that " circuit 16 of Hamaguchi et al. is equivalent to the power interruption circuitry claimed by the applicant." Hamaguchi's CRT protection circuit utilizes an overvoltage/overcurrent detector 30 and control circuit 40 to control the turning off a horizontal output transformer Qa "**instantaneously**" upon detection of an abnormal state. See col. 2, lines 40-47. Circuit 16 of Hamaguchi is merely a rectifier that rectifies the high voltage output from transformer 15 before passing the high voltage on to the anode of the CRT, and has no other function. Circuit (rectifier) 16 is, therefore, **not** equivalent to the *power interruption delay charging means* claimed by the applicant. Accordingly, neither the Applicant's admitted prior art nor Hamaguchi teach or suggest ***gradually*** *lowering an input voltage*, and the Examiner has not provided a *prima facie* showing that one of ordinary skill in the art would have been motivated to provide *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.*

As noted above, the Examiner has **not** provided any sound scientific reasoning nor logical explanation of how the combination of references teach the feature of *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.* Instead, the Examiner erroneously suggests equivalency with respect to the Applicant's claimed *power interruption delay charging means* and circuit 16 of Hamaguchi, which is a rectifier, not a CRT protection circuit, that rectifies the current output from a flyback transformer to obtain a high voltage (HV). Hamaguchi does not describe rectifier 16 as having the function of *gradually lowering said input voltage to said H/V*

processor constant voltage circuit when power supplied to said display device is interrupted. At no point does the Examiner provide any logical explanation nor scientific reasoning to support the rejection. Instead, the Examiner has merely suggested using Hamaguchi's power regulatory circuitry with Applicant's admitted prior art "because it would protect the CRT display" without any explanation of how Hamaguchi's power regulatory circuitry would be made to perform the function of *gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted*

Assuming, *arguendo*, that on of ordinary skill in the art desired to modify the Applicant's admitted prior art using the teachings of Hamaguchi, there has been no showing that one would have been motivated to use rectifier 16 of Hamaguchi since rectifier 16 is not a protection circuit described by Hamaguchi. Clearly, Hamaguchi discloses that the protection circuit comprises rectifier 16, detector 22, overvoltage/overcurrent detector 30, cutoff transistor Qb **and** control circuit 40. Accordingly, in combining the Applicant's admitted prior art and Hamaguchi, one of ordinary skill in the art would have connected Hamaguchi's protection circuit as taught by Hamaguchi such that the cut off transistor Qb would have been connected to, for example, the base of transistor TR of horizontal output circuit 134 (Applicant's Figs. 1 and 2). There is no suggestion found in any of the applied art, which would have motivated one of ordinary skill in the art to provide a power interruption delay charging means for ***gradually lowering said input voltage to said H/V processor constant voltage circuit*** when power supplied to said display device is interrupted.

Accordingly, the rejection of claim 1 is deemed to be in error because circuit 16 of Hamaguchi **is not** equivalent to the claimed *power interruption delay charging means for gradually*

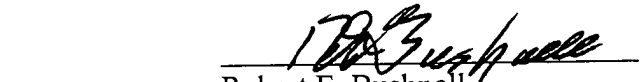
lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted; and the rejection should not be sustained.

IX. SUMMARY

As noted above, the issue is not one of "motivation to combine," but is instead one of whether the claim, as a whole, is taught by the combined prior art. Since the art fails to teach the **whole** feature of *power interruption* ***delay charging means*** *for* ***gradually lowering said input voltage to said H/V processor constant voltage circuit*** *when power supplied to said display device is interrupted,* then the rejection is in error.

Accordingly, the rejection of claims 1-4 is deemed to be in error and should not be sustained.

Respectfully submitted,



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X. APPENDIX

CLAIMS UNDER APPEAL

1. A display device with a power interruption delay function, comprising:

a pulse width modulation controller for generating a pulse width modulation signal under the control of a microcomputer;

a current amplifier for amplifying current in response to the pulse width modulation signal from said pulse width modulation controller;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

a horizontal deflection coil for horizontally deflecting electron beams generated in said display device;

an S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver;

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to an input voltage; and

power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

2. The display device as set forth in claim 1, wherein said power interruption delay charging means includes:

a polarity capacitor for performing a charging operation when power is supplied to said display device and a discharging operation when the power supplied to said display device is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supplied to the display device is interrupted.

3. A display device with a power interruption delay function, comprising:

a power supply circuit for converting a received commercial AC power into a DC input voltage;

a horizontal deflection circuit under the control of a microcomputer, receiving said DC input voltage, for horizontally deflecting electron beams generated in said display device; and

power interruption delay charging means for gradually lowering said DC input voltage received by said horizontal deflection circuit when said AC power supplied to said power supply circuit is interrupted, said power interruption delay charging means comprising:

a polarity capacitor for performing a charging operation when said AC power

is supplied and a discharging operation when said AC power is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to said power supply circuit when said AC power is interrupted.

4. The display device as set forth in claim 3, wherein said horizontal deflection circuit comprises:

a pulse width modulation controller for generating a pulse width modulation signal under the control of said microcomputer;

a current amplifier for amplifying current in response to said pulse width modulation signal generated by said pulse width modulation controller;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

a horizontal deflection coil for horizontally deflecting said electron beams;

a S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver; and

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to said DC input voltage, said DC input voltage being received through said power interruption delay charging means.